DSI Aerospace Technology

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DSI Aerospace Technologie GmbH • Otto-Lilienthal-Str. 1
D-28199 Bremen • Germany
Phone +49 421 596969-31
Fax +49 421 596969-59
http://www.dsi-as.de

Master's Thesis

Design and implementation of a space-qualified RISC-V-based wireless communication system

High-performance satellite communications are a major challenge considering the design of modern space applications and systems. In contrast to the traditional radio transmission approaches that are based on unprogrammable and –configurable static ICs, modern hardware platforms allow the flexible definition of all the necessary physical layer components, e.g. (de-)modulators, de-/encoders, etc. A promising trade-off between flexibility and performance can be achieved by the use of high-end application-specific instruction set processors (ASIPs) that possess a programmable CPU but also application optimized instructions.

During the last years, the RISC-V processor has become an interesting alternative to the expensive existing IP-cores. Right now, there are several ongoing research activities and developments targeting a different design goals between the high-performance and low-power antipodes. Moreover, most of these cores offer the possibility to add application-specific extensions to the instruction set as well as integrating new hardware accelerator peripherals. Hence, RISC-V-based cores are a promising platform for software-/hardware-based signal processing in the baseband.

Task Description

Main goal of the Master's Thesis is to design a RISC-V-based wireless signal processing chain for state-of-the-art satellite-ground communication systems. In detail, this work comprises

- Getting familiar with the basic ideas of well-established wireless communication technologies (MIMO, OFDM/GFDM) and signal processing blocks (de-/encoder, channel equalization/estimation,…)
- Design of a C/C++-based RISC-V wireless communication transmitter/receive path
- Selection of an appropriate RISC-V platform for FPGA mapping
- Software Verification/Testing on a RISC-V evaluation board
- Implementation of a FPGA-based Verification Framework and basic testing

Prerequisites

- Basic knowledge of **FPGA design and/or VHDL/Verilog**
- Basic knowledge of **wireless communications**
- Basic knowledge of **C/C++**
- Basic knowledge of **programmable architectures**

Contact

Dr. Jochen Rust **DSI Aerospace Technologie GmbH** **Phone: +49 421 596969-31** **jochen.rust@dsi-as.de**